

Wearable Brainwave Processor

— Power Management Kit Development

➤ Project description

The Electronic Systems (ES) group is going to initiate a large project which is going to develop an ultra-low power brainwave processor. This brainwave processor is going to be integrated in a wearable brainwave processing platform for 24-hour/7-day healthcare of patients with epilepsy and Parkinson's disease in non-hospital environments. To achieve 24/7 continuous monitoring, a variety of ultra-low power design methodologies have to be developed.

STMicroelectronics 28nm FDSOI CMOS technology, which is the most advanced CMOS technology available in academia, will be used for the development of the brainwave processor. Since this 28nm technology is still new to both academia and industry, the IP's available in this technology still far lag behind the requirement of users. In order to fully exploit the capability of this 28nm technology to achieve both high performance and ultra-low power consumption, certain IP's have to be developed beyond the standard cell library that is available by STMicroelectronics. The focus of this project will be the development of power management kit for the STMicroelectronics 28nm FDSOI CMOS technology.

➤ What you are expected to do

In this project, you are expected to develop a complete power management kit for STMicroelectronics 28nm FDSOI CMOS technology. This design kit should include sleep transistors, data retention flip-flops, level shifters, and isolation cells. Transistor-level design, optimization, and simulations will be used extensively with the aid of Cadence EDA tools. Furthermore, Cadence Liberate will be used for the characterization of your designed cells and the generation of library files (that will be used for logic synthesis, placement and routing, etc.). With your designed power management kit, you are also required to implement low power techniques, such as power gating, multiple power domain, and voltage scaling, with an ARM Cortex-M0 processor. You need to go through logic synthesis, placement and routing, and timing/power/signal integrity signoff with the M0 processor, the STMicroelectronics 28nm standard cell library, as well as your newly developed power management kit.

➤ What you get

1. Two supervisors:
 - Prof. José Pineda de Gyvez, Electronic Systems, TU/e / NXP Semiconductors (IEEE Fellow / NXP Fellow)
 - Dr. Hailong Jiao, Electronic Systems, TU/eYou will have the access to both academic and industrial design and test experience.
2. Access to a variety of state-of-the-art EDA tools from Cadence and advanced CMOS technologies.
3. Very good chance to publish one IEEE conference paper.
4. Possibility to be involved in the tape-out of a chip.

➤ Project duration

Final project (six to nine months).

➤ Contact

If you are interested, please send an email to Dr. Hailong Jiao (h.jiao@tue.nl).