Technische Universiteit Eindhoven University of Technology
Where innovation starts

Electronic Systems

Wearable Brainwave Processor

— Design flow exploration for ARM Cortex-M0

➢ Project description

The Electronic Systems (ES) group is going to initiate a large project which is going to develop an ultra-low power brainwave processor. This brainwave processor is going to be integrated in a wearable brainwave processing platform for 24-hour/7-day healthcare of patients with epilepsy and Parkinson's disease in non-hospital environments. To achieve 24/7 continuous monitoring, a variety of ultra-low power design methodologies have to be developed.

ARM Cortex-M0 is the most commonly used microprocessor in low-power systems. Cortex-M0 will be embedded in our brainwave processor as a general-purpose CPU core to achieve high reconfigurability. STMicroelectronics 28nm FDSOI CMOS technology will be used for the development of the brainwave processor. The physical design of Cortex-M0 with such advanced CMOS technology is a great challenge, especially if ultra-low power consumption is the target.

➢ What you are expected to do

In this project, you are expected to develop the whole design flow for ARM Cortex-M0, from logic synthesis all the way to tape-out, with the STMicroelectronics 28nm FDSOI CMOS technology. With the existing HDL code of Cortex-M0, you need to go through logic synthesis, placement and routing, and timing/power/signal integrity signoff. You are also required to integrate SRAM macros into the M0 core. I/O pads are required to be placed in the final layout which is ready for tape-out. With the complete layout, you are required to use existing compiler and write C-code benchmarks (or use existing benchmarks) to bootstrap and exercise the platform.

➢ What you get

1. Two supervisors:
➢Prof. José Pineda de Gyvez, Electronic Systems, TU/e / NXP Semiconductors (IEEE Fellow / NXP Fellow)
➢Dr. Hailong Jiao, Electronic Systems, TU/e
You will have the access to both academic and industrial design and test experience.
2. Access to a variety of state-of-the-art EDA tools from Cadence and advanced CMOS technologies.
3. Very good chance to publish one IEEE conference paper.
4. Possibility to be involved in the tape-out of a chip.

➢ Project duration

Final project or internship (dependent on your background).

➢ Contact

If you are interested, please send an email to Dr. Hailong Jiao (h.jiao@tue.nl).