Technische Universiteit Eindhoven University of Technology
Where innovation starts

Electronic Systems

Wearable Brainwave Processor

— Low-Noise MTCMOS Circuits with Timing/Energy-Efficient Mode Transitions

➢ Project description

The Electronic Systems (ES) group is going to initiate a large project which is going to develop an ultra-low power brainwave processor. This brainwave processor is going to be integrated in a wearable brainwave processing platform for 24-hour/7-day healthcare of patients with epilepsy and Parkinson's disease in non-hospital environments. To achieve 24/7 continuous monitoring, a variety of ultra-low power design methodologies have to be developed.

MTCMOS, also known as power/ground gating, is the most commonly used circuit technique for leakage power reduction. An integrated circuit is typically divided into multiple autonomous power/ground gating domains for effective reduction of leakage power consumption. With more frequent transitions between the ACTIVE and SLEEP modes of operation to achieve more effective leakage power savings, reactivation noise has become an important reliability concern in modern integrated circuits. The timing and energy consumed during mode transitions is also an important concern in MTCMOS circuits. Lower mode transition timing overhead and energy consumption enable an MTCMOS circuit to transition to SLEEP mode more frequently, thereby allowing more significant leakage power savings. MTCMOS circuit techniques with suppressed mode transition noise, timing overhead, and energy consumption are therefore highly desirable.

➢ What you are expected to do

In this project, you are expected to develop a next-generation mode transition strategy for MTCMOS circuits. The proposed technique is expected to be used extensively in the brainwave processor. You will need to synthesize different techniques, such as sleep signal modulation and charge recycling, to achieve aggressive reduction in mode transition noise, timing overhead, and energy consumption in MTCMOS circuits. You will also need to integrate the new idea into the standard digital IC design flow with a series of Cadence tools.

➢ What you get

1. Two supervisors:
➢Prof. José Pineda de Gyvez, Electronic Systems, TU/e / NXP Semiconductors (IEEE Fellow / NXP Fellow)
➢Dr. Hailong Jiao, Electronic Systems, TU/e
You will have the access to both academic and industrial design and test experience.
2. Access to a variety of state-of-the-art EDA tools from Cadence and advanced CMOS technologies.
3. Very good chance to publish one or two IEEE conference/journal papers.
4. Possibility to be involved in the tape-out of a chip.

➢ Project duration

Final project or internship (dependent on your background).

➢ Contact

If you are interested, please send an email to Dr. Hailong Jiao (h.jiao@tue.nl).