

Wearable Brainwave Processor

— Accuracy-Adjustable Energy-Efficient Approximate Classifier

➤ Project description

The Electronic Systems (ES) group is going to initiate a large project which is going to develop an ultra-low power brainwave processor. This brainwave processor is going to be integrated in a wearable brainwave processing platform for 24-hour/7-day healthcare of patients with epilepsy and Parkinson's disease in non-hospital environments. To achieve 24/7 continuous monitoring, a variety of ultra-low power design methodologies have to be developed.

In a variety of application domains, such as image processing, pattern recognition, or accuracy non-critical signal processing, the accuracy of the computed results can be degraded to a particular extent without sacrificing the quality-of-service or the quality-of-experience. Substantial possibilities therefore become available for optimizing the power consumption of approximate circuits. Approximate computing is therefore emerging as a new low power design paradigm in the nanometer regime. The processing of brainwave signals, such as feature extraction and classification, is a statistical process which provides approximate results. Due to the built-in statistical and approximate property of brainwave processing, approximate computing can be naturally utilized for significant energy savings with little classification accuracy loss. Support Vector Machine (SVM) is one of the most commonly used classifiers for brainwave processing. The target of this project is to implement SVM classifier in HDL codes by using approximate arithmetic circuits.

➤ What you are expected to do

In this project, you are expected to implement SVM classifier in HDL code. The arithmetic circuits, such as adders and multipliers, need to be implemented in both accurate versions and approximate versions. The accuracy of the SVM classifier should be able to be adjusted by tuning particular parameters in the approximate arithmetic circuits. With your HDL codes, you are also required to go through logic synthesis, placement and routing, and timing/power/signal integrity signoff for the SVM classifier by using Cadence EDA tools. The accuracy of the classifier needs to be verified with both Matlab and logic simulations. The tradeoff between accuracy and power/energy consumption of the classifier needs to be analyzed.

➤ What you get

1. Two supervisors:

➤ Prof. José Pineda de Gyvez, Electronic Systems, TU/e / NXP Semiconductors (IEEE Fellow / NXP Fellow)

➤ Dr. Hailong Jiao, Electronic Systems, TU/e

You will have the access to both academic and industrial design and test experience.

2. Access to a variety of state-of-the-art EDA tools from Cadence and advanced CMOS technologies.

3. Very good chance to publish one or two IEEE conference/journal papers.

4. Possibility to be involved in the tape-out of a chip.

➤ Project duration

Final project (six to nine months).

➤ Contact

If you are interested, please send an email to Dr. Hailong Jiao (h.jiao@tue.nl).